

How to Successfully Calibrate an Open-Loop DAC Signal Chain

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Introduction

Any practical electronic application is subject to multiple sources of error that can make the most precise components deviate from their data sheet behavior. When the application signal chain doesn't have a built-in mechanism to self-adjust for these errors, the only approach to minimize their impact is to measure them and calibrate them out systematically.

An open-loop system is a system that does not use its output to perform adjusting control actions on its inputs to achieve the required performance, while in a closed-loop system, the output depends on a control action in the system that can automatically implement corrections to improve performance. Most digital-to-analog converter (DAC) signal chains are set-and-forget type systems, where the accuracy of the output must rely on the accuracy of each block in the signal chain. A set-and-forget system is an open-loop system. For an open-loop system that requires high accuracy, calibration is most likely needed and recommended.

We'll introduce two types of DAC signal chain calibration: the TempCal (calibration at operating temperature), which can give the best level of error correction, and the SpecCal (calibration using specifications), which is a valid alternative when using TempCal is not possible, but it's not as comprehensive.

Table 1. Calibration Types and Errors That Can Be Corrected

	TempCal	SpecCal
DAC Intrinsic Errors	✓	✓
Key Components Intrinsic Errors	✓	Can be included (for example, V_{REF})
Other System-Level Errors	✓	x

Type of DACs

A unipolar voltage DAC can only give output either of positive or of negative. This article will look at the [AD5676R](#) as an example of a unipolar DAC and how to accurately calibrate it. The same approach can be used to make necessary adjustments with other types of DACs.

Bipolar voltage DACs like the [AD5766](#) can achieve both positive and negative output.

Current-output DACs are typically used in a multiplying configuration (MDAC) to provide variable gain; they usually require external amplifiers to buffer the voltage generated across a fixed resistor.

Precision current sourcing DACs (IDACs), like the [AD5770R](#) and the [LTC2662](#), are a new category of DACs that can precisely set an output current in a predefined range without requiring any additional external component.

DAC Transfer Function Theory and Intrinsic Errors

An ideal digital-to-analog converter produces an analog output voltage or current exactly proportional to the input digital code and independent of unwanted external influences like power supplies and reference variations.

For an ideal voltage output DAC, the increase in output for a single step increase in input digital code is called LSB and is defined as:

$$LSB_{SIZE}(V) = \frac{(V_{REF+}) - (V_{REF-})}{2^n - 1} \quad (1)$$

where:

(V_{REF+}) and (V_{REF-}) are the positive and negative reference voltage. In some cases, (V_{REF-}) is equal to ground (0 V).

n is the resolution of the DAC in bits.

$LSB_{SIZE}(V)$ is the smallest increment to the DAC output in volts.

This means that for any given input code, once the LSB is known, it should be possible to accurately predict the voltage output of the DAC.

$$V_{OUT}(V) = DAC\ Code \times LSB_{SIZE}(V) \quad (2)$$

In practice, the accuracy of the DAC output is subject to gain and offset errors from the DAC (intrinsic errors) and other components in the signal chain (system-level errors). For example, some DACs have an integrated output amplifier, while others require one that then becomes a possible source of additional errors.

In data sheets, the most relevant specifications are defined in the terminology section. For DACs, this section lists parameters like offset error and gain error.

Zero-scale error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register.

Figure 1 shows how offset and gain errors affect a DAC transfer function for a unipolar voltage DAC.

Gain error is a measurement of the span error of the DAC, shown in purple in Figure 1. The gain error is the deviation in slope of the DAC transfer characteristic from the ideal. The ideal DAC transfer is shown in black.

Offset error is a measurement of the difference between the actual and ideal output, in the linear region of the transfer function, shown in blue in Figure 1. Note that the transfer function in blue is interpolated to meet the y-axis for negative V_{OUT} and identify the offset error.

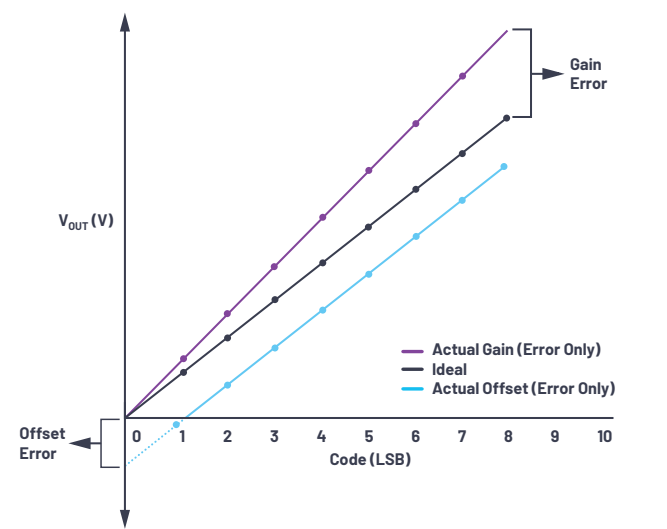


Figure 1. Representation of offset error and gain error for a unipolar DAC.

The effect of both gain error and offset error can be seen in the blue plot of Figure 4.

The same parameters are also defined in relation to how they change (drift) with changes in temperature.

Zero code error drift is a measure of the change in zero code error with changes in temperature.

The gain error temperature coefficient is a measurement of the change in gain error with changes in temperature.

Offset error drift is a measurement of the change in offset error with a change in temperature.

Temperature variation plays a major role in the accuracy of electronic systems. While the intrinsic gain and offset error of a DAC are usually specified with respect to temperature, there are other components of the system that can have an impact on the overall offset and gain of the output.

So even when the INL and DNL of the DAC are very competitive, there are other errors to consider—particularly with respect to temperature. Most recent DACs specify the total unadjusted error (TUE) as a measure of the output error taking all the various errors into account—namely, INL error, offset error, gain error, and output drift over supplies and temperature. TUE is expressed in %FSR.

When the data sheet doesn't specify TUE for a DAC, it can be calculated using a technique called RSS, or root sum squared—a technique used to sum uncorrelated error sources for error analysis.

$$TUE = \sqrt{INL_{ERR}^2 + Offset_{ERR}^2 + Gain_{ERR}^2 + \dots} \tag{3}$$

There are other, smaller error sources that are usually omitted because of their less relevant contribution like output drift, etc.

Each of the specifications of each component in the system must be converted into the same units. This can be done using Table 2.

Table 2. Units Conversion Matrix

	LSB	Volts	%FSR	PPM
LSB		$LSB/2^N \times V_{REF}$	$LSB/2^N \times 100$	$LSB/2^N \times 10^6$
Volts	$(V \times 2^N)/V_{REF}$		$V/V_{REF} \times 100$	$V/V_{REF} \times 10^6$
%FSR	$(\%FSR)/100 \times 2^N$	$\%FSR/100 \times V_{REF}$		$\%FSR \times 10^4$
PPM	$PPM/10^6 \times 2^N$	$PPM/10^6 \times V_{REF}$	$PPM/10^4$	

TUE is a great asset to succinctly explain how accurate the DC DAC output is as a result of the sum of the intrinsic errors; however, it does not factor in system-level errors that differ depending on the signal chain the DAC is implemented in and its environment.

It's worth noting that some DACs have a built-in buffer/amplifier in the output stage and the data sheet specifications in this case reflect the effects of both as part of the intrinsic errors.

System-Level Errors

When trying to analyze a DAC signal chain error budget for a given application, the system designer should consider and verify the different components' contributions, paying attention to the temperature at which the system is expected to operate. Depending on the final applications, there can be many different building blocks to the signal chain, including power ICs, buffers or amplifiers, and different types of active loads that can contribute to the system-level errors.

Reference Source

Every DAC requires a voltage reference to operate from. The reference source is one of the major contributors to the accuracy of the DAC and of the overall signal chain.

The key reference performance specifications are also defined in standalone reference data sheets like the [ADR45xx family](#) or as part of the DAC data sheet if the device has an internal reference source available to the user.

Dropout voltage, sometimes referred to as supply voltage headroom, is defined as the minimum voltage differential between the input and output such that the output voltage is maintained to within 0.1% accuracy.

The temperature coefficient (TC or TCV_{OUT}) relates the change in the output voltage to the change in the ambient temperature of the device, as normalized by the output voltage at 25°C. The TCV_{OUT} for the [ADR4520/ADR4525/ADR4530/ADR4533/ADR4540/ADR4550](#) A grade and B grade is fully tested over three temperatures: -40°C, +25°C, and +125°C. The TCV_{OUT} for the C grade is fully tested over three temperatures: 0°C, +25°C, and +70°C. This parameter is specified using two methods. The box method is the most common method and accounts for the temperature coefficient over the full temperature range, whereas the bowtie method calculates the worst-case slope from +25°C and is therefore more useful for systems that are calibrated at +25°C.

For certain DACs, external reference sources exhibit better performance compared to integrated references. The reference voltage directly impacts the transfer function, so any change in this voltage proportionally changes the slope of the transfer function—that is, the gain.

It's worth noting that some DACs have a built-in buffered internal reference and the data sheet specifications in this case reflect the effects of these internal blocks as part of the intrinsic errors.

Line Regulation

Line regulation is defined for every standalone IC acting as a supply as the change in output in response to a given change in input. This applies to the power supply, buffers, and reference ICs that are supposed to maintain their output voltage stable regardless of the input. Line regulation is usually specified in data sheets at ambient temperature.

Load Regulation

Load regulation is defined as the incremental change in output voltage for a change in load current. Voltage outputs are usually buffered to reduce the impact of this variation. Some DACs may not buffer the reference input. Therefore, as the code changes, the reference input impedance will also change, causing a change in reference voltage. The effect on the output is generally small but should be considered in high accuracy applications. This is usually specified in data sheets at ambient temperature.

Solder Heat Resistance Shift

Solder heat resistance (SHR) shift is particularly relevant to reference source. It refers to the permanent shift in output voltage that is induced by exposure to reflow soldering and is expressed as a percentage of the output voltage. See the data sheets for the ADR45xx family for more details. In general, all ICs are somehow affected by the SHR shift, but this is not always quantifiable, and it depends greatly on the specific system assembly for the application.

Long-Term Stability

Long-term stability defines the change in output voltage vs. time and is specified in ppm/1000 hours. An application's long-term stability can be improved by PCB-level burn-in.

Open-Loop Calibration Theory

A DAC signal chain simplified diagram is shown in Figure 2. The blocks outlined in black show a simplified open-loop signal chain, while those outlined in gray are an example of the additional components needed to realize the closed-loop signal chain.

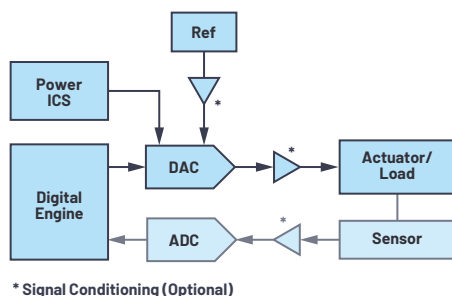


Figure 2. DAC signal chain simplified diagram.

The closed-loop option requires additional components and digital data manipulation via software to deliver a much more accurate output. When these additional resources can't be added for various reasons (space, cost, etc.), the open-loop solution is still valid—provided it can deliver the required accuracy. That's where this article can help in clarifying how the open-loop calibration can be done.

Calibrating out gain and offset errors that are constants with no external influences is a simple procedure in theory. The linear region of the transfer function of the DAC can be modeled as a straight line described by:

$$y = mx + c \quad (4)$$

where:

y is the output.

m is the slope of the transfer function accounting for the gain error (shown in purple in Figure 1).

x is the input to the DAC.

c is the offset voltage (shown in blue in Figure 1).

Ideally m is always one and c is always zero. In practice they account for the gain and offset error of the DAC and, once known, they can be accounted for in the DAC input to achieve a number closer to the ideal DAC output. The gain can be calibrated out by multiplying the digital DAC input by the reciprocal of the gain error. The offset error can be removed by adding the inverse of the measured offset error to the digital DAC input.

The equation below shows how to calculate the correct DAC input to produce the desired voltage:

$$\text{Actual DAC Code} = \frac{\text{Ideal DAC Code}}{\text{Gain}} - \text{Offset Error (LSB)} \quad (5)$$

where:

$$\text{Gain} = \frac{\text{Actual Output Span}}{\text{Ideal Output Span}} \quad (6)$$

$$\text{Offset Error (LSB)} = \frac{\text{Offset Error (V)}}{\text{LSB}_{\text{SIZE}} \text{ (V)}} \quad (7)$$

Note that offset error can be positive or negative.

Also see the "Open-Loop Calibration Techniques for Digital-to-Analog Converters" Analog Dialogue article.

How to Successfully Calibrate a DAC Signal Chain

In this section we'll describe how to calibrate offset and gain in a DAC signal chain in practice, using the AD5676R as an example. For all the measurements, the EVAL-AD5676 evaluation kit has been used with the AD5676R internal reference enabled. The EVAL-AD5676 board and the measurement setup are both part of the signal chain we are measuring in the example. Each component of this signal chain (power ICs on the board, AD5676R, parasitics introduced by layout and connectors, etc.) is contributing to the system errors. The idea is to show how this system can be calibrated as an example for any other system of choice.

An EVAL-SDP-CB1Z Blackfin® SDP controller board (SDP-B) is used to communicate with the AD5676R on the EVAL-AD5676 evaluation kit and an 8-digit DMM is used to measure the output voltage of $V_{\text{OUT}0}$. A climate chamber is used to control the temperature of the full system made of EVAL-SDP-CB1Z plus EVAL-AD5676 with the AD5676R using the internal reference.

The EVAL-AD5676 is powered up as described in the User Guide and the link configuration is shown in Table 3.

Table 3. Configuration of Jumpers on EVAL-AD5676 Board for Described Measurements

Link No.	Position
LK1	A
LK2	A
LK3	A
LK4	A

First the signal chain errors without calibration (NoCal) have been assessed for different temperatures. The output error has been calculated considering the difference in LSBs between the ideal value and the measured value at specific input codes. This error includes both the intrinsic and extrinsic errors of the DAC and the overall signal chain on the EVAL-AD5676 board. The output error with no calibration is shown in Figure 3.

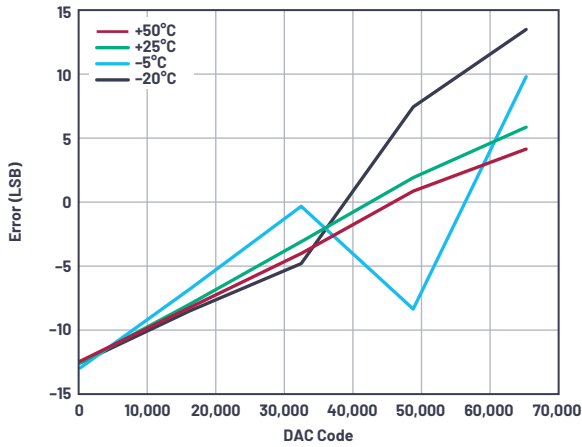


Figure 3. EVAL-AD5676 output error in LSB with NoCal.

The information needed to calculate the offset and gain errors and, subsequently, the correction codes resides in the transfer function. Two points are needed for that: one data point close to zero-scale (ZS_{LIN}) and one close to full-scale (FS_{LIN}). The idea is to work in the linear region of the DAC. This information is usually provided together with INL and DNL specs, most likely in the endnotes to the spec table. For the AD5676R, for example, the linear region goes from code 256 and code 65280.

Figure 4 shows a diagram to explain the linear region of a DAC.

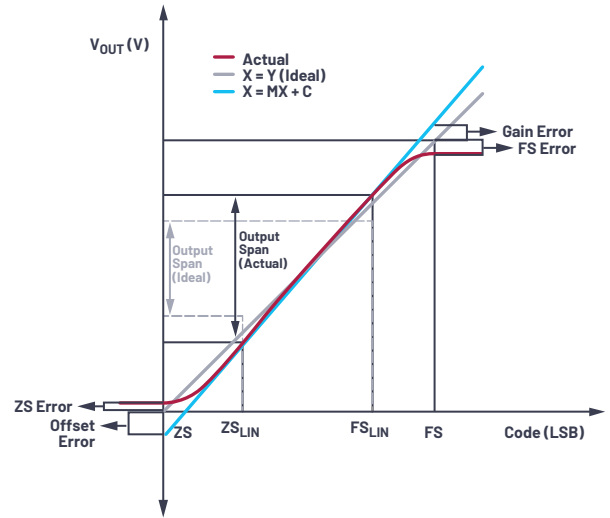


Figure 4. Unipolar voltage DAC transfer function and errors.

Once the ZS_{LIN} and FS_{LIN} codes have been identified, we can collect the measurements needed for the calibration, which are the DAC voltage outputs at those two codes (V_{OUT} at ZS_{LIN} and V_{OUT} at FS_{LIN}), plus a few other codes in between ($1/4$ scale, mid-scale, and $3/4$ scale)

The measurements should be collected at the operating temperature for the application. When this is not possible, the data sheets of the devices in the signal chain can be used to derive the information needed, once the two main data points have been collected at ambient.

Each device in the signal chain contributes to the errors, and each board is different from the other, so it should be calibrated individually.

TempCal: Calibration at Operating Temperature

The best level of calibration is achieved by measuring the errors in the application environment at the operating temperature, and systematically correcting them when writing to the DAC to update the output.

To calibrate the DAC using this method, at the temperature the system will be operating at, measure the DAC output at code ZS_{LIN} and FS_{LIN} . Construct the transfer function as follows:

$$V_{OE} = \text{Actual Output at } ZS_{LIN} - \text{Ideal Output at } ZS_{LIN} \quad (8)$$

$$\text{Actual Output Span} = V_{FS,LIN,ACT} - V_{ZS,LIN,ACT} \quad (9)$$

$$\text{Ideal Output Span} = V_{FS,LIN,IDEAL} - V_{ZS,LIN,IDEAL} \quad (10)$$

$$\text{Gain} = \frac{\text{Actual Output Span}}{\text{Ideal Output Span}} \quad (11)$$

$$\text{LSB} = \frac{\text{Actual Output Span}}{FS_{LIN} - ZS_{LIN}} \quad (12)$$

$$\text{Actual Code} = \frac{\text{Ideal Code}}{\text{Gain}} - \frac{V_{OE}}{\text{LSB}} \quad (13)$$

where:

V_{OE} = Offset error (V)

$V_{FS,LIN,ACT}$ = Actual output at FS_{LIN}

$V_{ZS,LIN,ACT}$ = Actual output at ZS_{LIN}

$V_{FS,LIN,IDEAL}$ = Ideal output at FS_{LIN}

$V_{ZS,LIN,IDEAL}$ = Ideal output at ZS_{LIN}

Note that offset error can be positive or negative.

Figure 5 shows the output error achieved for the EVAL-AD5676 evaluation kit with the TempCal method.

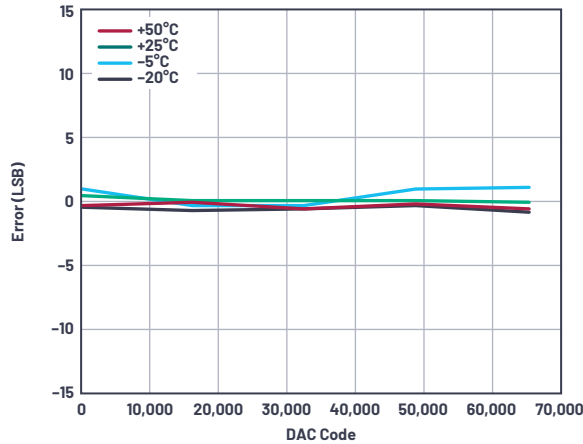


Figure 5. System output error in LSB with TempCal at different temperatures.

SpecCal: Calibration Using Specifications

If it is not possible to measure the errors in the application environment at the operating temperature, it is still possible to achieve a high level of calibration using the AD5676R data sheet and the DAC transfer function calibrated at ambient temperature.

To calibrate the DAC using this method, measure the DAC output at codes ZS_{LIN} and FS_{LIN} at ambient temperature. Construct the transfer function as described in the TempCal section by calculating the gain and offset error at ambient and applying Equation 14.

$$Actual\ Input = \frac{Ideal\ Input}{GE_{amb}} - \frac{V_{OE,amb}}{LSB} \quad (14)$$

where:

GE_{amb} = Gain error at ambient temperature

$V_{OE,amb}$ = Offset error (V) at ambient temperature

Calibrating the DAC signal chain at ambient temperature accounts for the system-level errors. However, the change of the external errors due to temperature change are not accounted for; thus, this method of calibration is not as accurate as the TempCal method.

Drift in intrinsic DAC errors, namely offset and gain errors, due to change in operating temperature can then be accounted for using the data sheet specifications. This is what we call SpecCal. The typical value of offset error drift is listed in the specifications table of the AD5676R data sheet, and the offset error vs. temperature typical performance characteristics (TPC) indicates which direction the error drifts depending on an increase or decrease in temperature from ambient.

$$V_{OE,drift} = Offset\ Error\ Drift \times \Delta Temperature \quad (15)$$

The change in gain error due to temperature is indicated in the gain error vs. the temperature TPC. Determine the gain error in % of FSR from the graph and apply Equation 16.

$$GE_{temp} = \frac{100 - \Delta Gain\ Error\ (TPC)}{100} \quad (16)$$

Now that we have estimated the offset error and gain error at the operating temperature, we can use Equation 17 to determine the input codes for the SpecCal output.

$$Actual\ Input = \frac{GE_{temp}}{GE_{amb}} \times \frac{Ideal\ Input - \frac{V_{OE,amb}}{LSB} - \frac{V_{OE,drift}}{LSB}}{LSB} \quad (17)$$

where:

$$\Delta Gain\ Error(TPC) = GE_{amb}(TPC) - GE_{temp}(TPC) \quad (18)$$

Figure 6 shows the output error achieved for the EVAL-AD5676 evaluation kit with the SpecCal method.

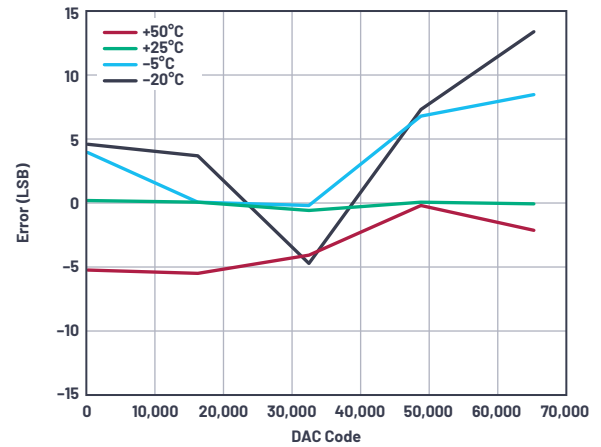


Figure 6. System output error in LSB with SpecCal at different temperatures.

The internal reference was used in this instance. An external reference can add to the overall error. Errors due to the reference source can be accounted for using the reference data sheet by considering the reference drift at the temperature of interest. Changes to the reference voltage alter the actual output span and, thus, the LSB size. This should be accounted for if an external reference is used. The temperature vs. output voltage TPC can be used to determine the change in the output span due to the reference drift.

$$\frac{Actual\ Output\ Span_{temp}}{Actual\ Output\ Span_{amb} + VREF_{drift}} = \quad (19)$$

where:

$$VREF_{drift} = VREF_{temp}(TPC) - VREF_{ideal} \quad (20)$$

Conclusion

This article outlined some of the main causes of error in a DAC signal chain, including DAC intrinsic errors that are defined in the data sheet and system-level errors that vary depending on the system and must be considered in an open-loop application.

Two methods of calibration have been discussed, one for when the DAC can be calibrated at the temperature the system will be operating at and the second for

when it is not possible to calibrate at the operating temperature, but measurements can be taken at ambient temperature instead. The second method uses the TPCs and the specifications outlined in the data sheet of the DAC and other ICs in the signal chain, to account for gain and offset error drift.

The TempCal method can achieve much better accuracy than the SpecCal one. For example, Figure 7 shows how, for the EVAL-AD5676 board at 50°C, the TempCal method achieved a level of accuracy very close to the ideal, while the SpecCal method still managed to deliver an improvement from the NoCal data.

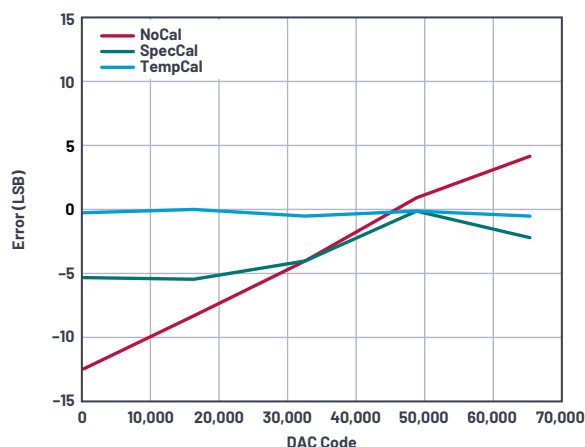


Figure 7. System output error in LSB with NoCal, SpecCal, and TempCal at 50°C.

Temperature variation plays a major role in the accuracy of electronic systems. Calibrating at the system operating temperature counteracts most errors. If this isn't possible, temperature variation can be tackled using the information available in the DAC and other ICs' data sheets to achieve accuracy of an acceptable degree.

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